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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/738,127	12/15/2000	Larry B. Li	50944.9900	9821

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EXAMINER
DEMAKIS, JAMES A

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 09/16/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/738,127	LI, LARRY B.	
	Examiner	Art Unit	
	James A Demakis	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *11* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. This application, filed under former 37 CFR 1.60, lacks formal drawings. The informal drawings filed in this application are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings. In unusual circumstances, the formal drawings from the abandoned parent application may be transferred by the grant of a petition under 37 CFR 1.182.

2. The drawings are objected to under 37 CFR 1.83(a) because they fail to show Cjs as described in the specification. Please note that the Examiner has assumed the Applicant is referring to a junction or parasitic Capacitance; but which one? Also, Sheet 6, line 11 compares Figure 1 to another Figure 1. It is unclear to the Examiner if there should be other Drawings with this Application. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. 35 U.S.C. 112, first paragraph, requires the specification to be written in "full, clear, concise, and exact terms." The specification is replete with terms which are not clear, concise and exact. The specification should be revised carefully in order to comply with 35 U.S.C. 112, first paragraph. Examples of some unclear, inexact or verbose terms used in the specification

are: page 3, unclear word; page 6, line 15, entire phrase is unclear, line 11, reference to Figure 1 (see comment in Drawing Section), line 9 , Cjs is not defined.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 2, 4-7, 9,10, 12-14, 16,17,19 rejected under 35 U.S.C. 103(a) as being unpatentable over Ravanelli, USPN 6,147,852 in view of Huard, USPN 4,875,130.

Regarding Claims 1, 2,4-7, 9,12-14,17,19;

Ravanelli(USPN 6147852) shows , as part of Figure 1, a "reverse mode" or reverse biased transistors Q1, Q2 connected in a diode configuration to form a "Zener" diode combination. Figure 2, further modifies on this principal, utilizing at least one bipolar transistor Q1 to shunt any ESD energy to a reference potential from an input circuit or a pad of a circuit to be protected, which may connect to an IC. This circuit differs from the claims in that the collector of this circuit is tied to a Supply line and the base is connected directly to Ground. Huard discloses an ESD protection circuit , Figures 4 and 5, which utilizes collector-emitter " break down" of a bipolar transistor 49 in response to current flowing across the reverse biased collector-base junction. The highest collector-emitter voltage breakdown is achieved when the base of the transistor is shorted to ground, and the lowest occurs when the base is left floating or

open. Ravanelli's circuit of Figure 2, is functionally equivalent to the device of the claims, but with the above stated differences. Ravanelli, also, does not disclose a transmission line coupling the source and the circuit to be protected. However, to one having ordinary skill in the art at the time of the invention, it would have been obvious to adjust the collector and base connection, as required to fit the design details of the bipolar transistor for the chosen breakdown levels and other operating characteristics; and it would also have been obvious to have considered the use of a transmission line structure when using high frequency circuits capable of performance above 2 GHz.

Regarding Claims 9,10,12, and 16;

Huard also treats and discloses typical breakdown voltages and operating voltages, see "Background of the Invention" and "Detailed Description" sections. Furthermore, it would appear straight forward to one of ordinary skill in the art that the voltage that the protection circuit begins to function has to be higher than the operating voltage of the circuit it is protecting; and the breakdown voltage of the protection transistor must be less than that of the following circuit requiring protection. For a protection transistor to operate at or near 5 volts would not be unusual, since most IC/ transistor circuits can operate at voltages below that, typically between 2-4 volts. For a person of ordinary skill in the art at the time of the invention, it would have been obvious to use 5 volts.

6. Claims 3,11, and 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Haas, Jr. et al (USPN 5,392,185) and in view of Ali (USPN 6,292,046).

Regarding Claims 3,11, and 15;

Haas, Jr et al discloses ESD protection circuits for RF applications using bipolar transistors and having improved characteristics of lower capacitance and high switching speeds, see "Summary of the Invention" and "Detailed Description of Preferred Embodiments", Section 3, lines 1-29. Ali discloses the limitations of ESD protection circuits above 100 MHz, in that for RF applications it is exceedingly important to minimize capacitive loading from the protection circuits, see "Background of the Invention" and "Summary of the Invention", Section 3,lines 1-36.

It would have been obvious to one having ordinary skill in the art at the time of the invention that Capacitive loading would have a detrimental effect on circuits operating above 1-2 GHz.

7. Claims 8 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haas, Jr. et al (USPN 5,537,284).

Regarding Claims 8 and 18;

Haas Jr et al discloses the use of PNP bipolar junction transistors in ESD protection circuits, see "Detailed Description of Preferred Embodiments", section 3, lines14-30 and section 5, line 56; and "Abstract".

It would have been obvious to one having ordinary skill in the art at the time of the invention that PNP transistors could be used in place of NPN transistors with adjustments for polarity differences.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James A Demakis whose telephone number is 703.305.7938. The examiner can normally be reached on 7:30AM-4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 703.308.3119. The fax phone numbers for the organization where this application or proceeding is assigned are 703.308.7722 for regular communications and 703.308.7721 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703.308.0956.

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September 5, 2002

Stephen W Jackson
9-9-02

STEPHEN W. JACKSON
PRIMARY EXAMINER